International Journal of Computer Applications (0975 – 8887)
Volume 104 – No.5, October 2014

Simulation Development of Carrier based Pulse Width Modulation for Cascaded Multilevel Inverter

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ABSTRACT
Cascaded multilevel inverter (CMLI) is emerging as a new breed of power converter options for high-power applications. Various topologies and modulation strategies of this inverter has been proposed. In this paper, Matlab simulink of CMLI using Carrier Based Pulse Width Modulation (CBPWM) techniques is developed to get optimum design and performances. Some parameter of this Simulink model can be varied, so some interesting characteristics of the inverter can be optimized. A simulation result shows that the system is easy and modular to adjust, and optimum performances can improve.

Keywords
cascaded multilevel inverter, carrier based pulse width modulation, frequency, total harmonic distortion

1. INTRODUCTION
Multilevel inverter (MLI) is an attractive choice of power electronic conversion for medium voltage and high-power applications in industries, because the output waveform has low harmonic content and can build using low voltage power electronic devices [1-3]. Various MLI topologies are discussed in the literatures. Cascaded, diode clamped and flying capacitor is famous topologies, but Cascaded MLI (CMLI) appears to be superior to another inverter topologies, because the modularity, and easy to control [4-6].

CMLI synthesizes a high or medium voltage output based on a series connection of power cells. The power qualities of these outputs depend on choice of modulation method. Carrier Based Pulse Width Modulation (CBPWM) is a simple method. This modulation uses a triangle carrier wave in each voltage level. To get triggers on each power device of H-bridge converter of CMLI, the carrier wave compare with sine wave reference [4-5]. The trigger signals appearance depends on amplitude, phase and frequency of the carrier wave.

In this paper, a Simulink Matlab circuit of CBPWM was developed for CMLI. This Simulink is made simple and modular, so the CBPWM parameters, like frequency and waveform of the carrier wave is easy to adjust to get optimal performance. Simulation model of CMLI 11 levels used to verify this system.

2. MODELLING
2.1. Cascaded Multilevel Inverter
CMLI constructed from a series connection of multiple H-bridge inverters. Each H-bridge consist a DC source and four power electronic devices, which have configured like a single-phase full-bridge inverter. By cascading the output voltages of each H-bridge inverter, a stepped voltage waveform is produced [4-5]. Fig. 1 shows a single-phase configuration of CMLI.

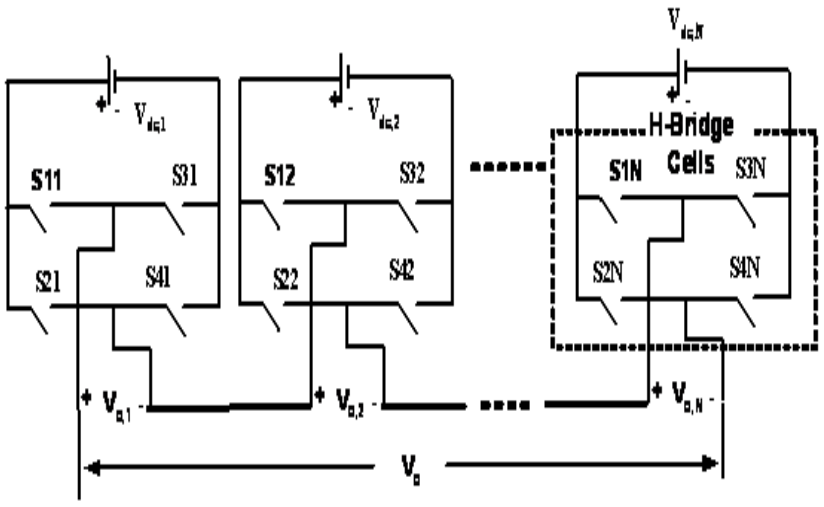


Fig. 1 Single-phase cascaded multilevel inverter

If each H-Bridge switches are S_{1N}, S_{2N}, S_{3N}, S_{4N}, and N is series of H-Bridges, so there are four relevant switching states in each H-Bridge as shown in Table 1 [5]. There are three output voltages which occurred, 0, V_{DCN} and $-V_{DCN}$. The 0 output must be chosen from two switching states happened. The voltage output of CMLI (V_o) obtained as sum of all output voltage on each H-Bridge. This output voltage is equal to Eq. (1) [6].

Table 1 Switches state and output voltage

Switches state				Output
S_{1N}	S_{2N}	S_{3N}	S_{4N}	
OFF	OFF	ON	ON	0
ON	ON	OFF	OFF	
ON	OFF	OFF	ON	V_{dcN}
OFF	ON	ON	OFF	$-V_{dcN}$

$$V_o(t) = V_{o,1}(t) + V_{o,2}(t) + ... + V_{o,N}(t) \qquad (1)$$

$$n = 2N+1 \qquad (2)$$

If V_{DCN} are equal voltage, the output voltage is equal to the equation (1). The number of CMLI levels can be predicted as twice of H-Bridge number used, plus one level, that is 0 levels. If the number of levels denoted n, so the relationship n and N are shown in equation (2).

2.2. Carrier Based Pulse Width Modulation
CMLI requires control to operate like Table 1 and to result output voltage like equation (1). This control called modulation. Among modulation methods, CBPWM is the most popular method. This method is easily implemented, because the principle of CBPWM is similar to a single sinusoidal pulse width modulation (SPWM), which uses a triangular carrier and sine reference to generate the trigger signal [5]. Fig. 2 shows the basic principle of SPWM [7-9]. In SPWM, sine wave (V_{MOD}) compare to triangle carrier wave (V_{TRIANG}) in the comparator, and produce trigger signal (V_{PWM}) for power electronic devices that is S_{1N}, S_{2N}, S_{3N}, and S_{4N}. Equation (3) shows these voltage relationships.

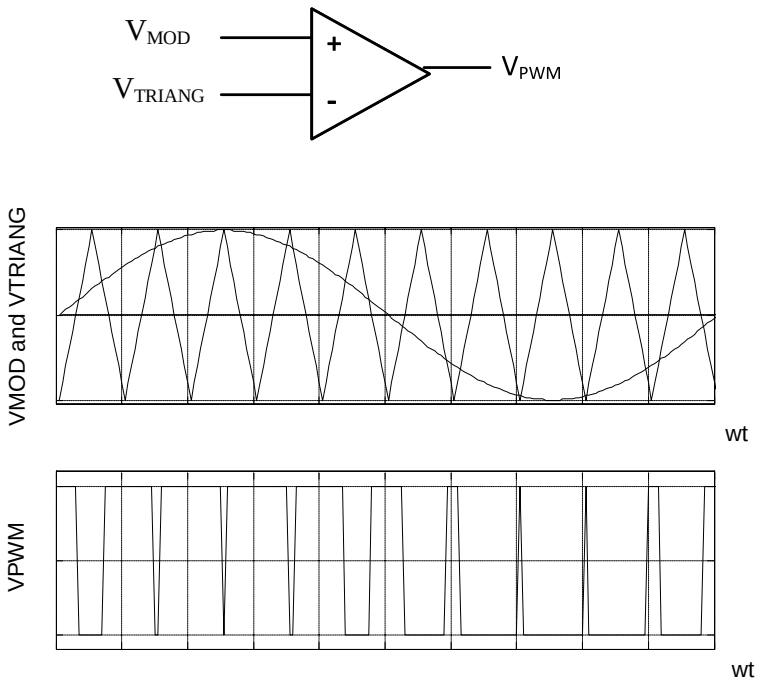
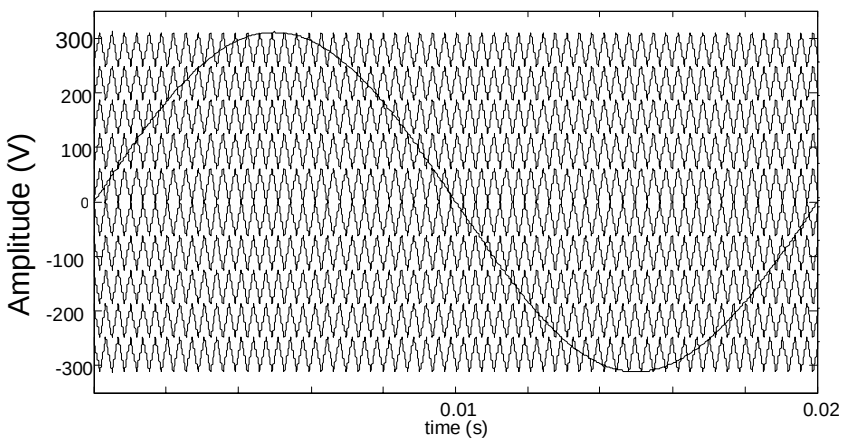
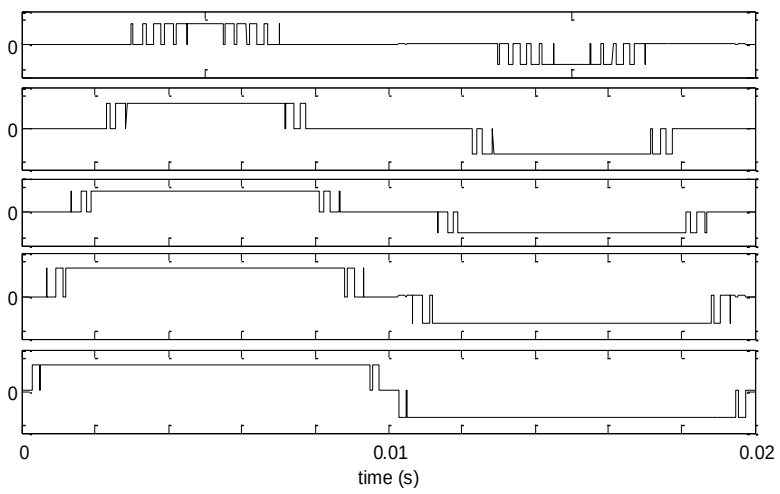


Fig. 2 Basic principle of PWM



(a) CBPWM input



(b) CBPWM output

Fig. 3 CBPWM for 11 levels

If $V_{MOD} > V_{TRIANG,}$ $V_{PWM} = 1$

If $V_{MOD} < V_{TRIANG,}$ $V_{PWM} = 0$ (3)

In the modulation, the amplitude modulation ratio or modulation index (m), and the frequency modulation ratio (p) are urgent parameters that influence the power quality. Formulation of these parameters is given by equation (4) and (5), where f_T is modulation frequency and f_S is triangle frequency.

$$m = \frac{V_{MOD}}{V_{TRIANG}} \quad (4)$$

$$p = \frac{f_T}{f_S} \quad (5)$$

CBPWM also uses triangle carrier and sine reference, but CBPWM use many triangle carriers. Each career should be biased to any voltage used. Fig. 3 show input signals and output signals of CBPWM for 11 levels. These output signals in Fig. 3 (b) produced by comparison between modulator (sine reference) and carriers (triangles) using equation (3) [5].

2.3. Analysis of Voltage Output Waveform

An analysis of CMLI output voltage can find using an example voltage output waveform in the single-phase as shown in Fig. 4 [9]. The output waveform is in the symmetrical pattern so only a quarter cycles drawn in the figure.

Fig. 4 shown, if the carrier frequencies increase, the number of pulses triggers also increase, vice versa if the frequencies decrease. So, the different frequencies also result the different pattern of output voltage, and will be influence of power quality. An optimum frequency needs to be found for the best power quality.

Fourier series expansion of this voltage can be expressed as the equation (6), where a_n and b_n is the Fourier coefficient [9]. This equation only produces odd function and in the symmetry pattern, the output voltage can be reduced to the equation (7). A generalized expression of b_n for any number of switching angles and any number of voltage levels is given in equation (8) [9].

$$v_{out} = \sum_{n=1}^{\infty}(a_n \cos n\theta + b_n \sin n\theta) \quad (6)$$

$$v_{out} = \sum_{1,3,5\ldots}^{\infty} b_n \sin n\theta \quad (7)$$

$$b_n = \frac{4V_{dc}}{n\pi}(V_1 \sum_{i=1}^{P_1}(-1)^i \cos n\alpha_i \pm V_2 \sum_{i=P_i+1}^{P_2}(-1)^i \cos n\alpha_i \pm \ldots\ldots \pm V_M \sum_{i=P_{M-1}+1}^{P_M}(-1)^i \cos n\alpha_i) \quad (8)$$

where

n = 1,3,5,....,2N-1

M = the number of dc sources

$P_1 = N_1$; $P_2 = N_1 + N_2$; ..... $P_M = N_1 + N_2 + \ldots + N_M$

N_1, N_2, ... N_M = the number of pulses per-quarter cycle at inverter

α_i = the i_{th} switching angle

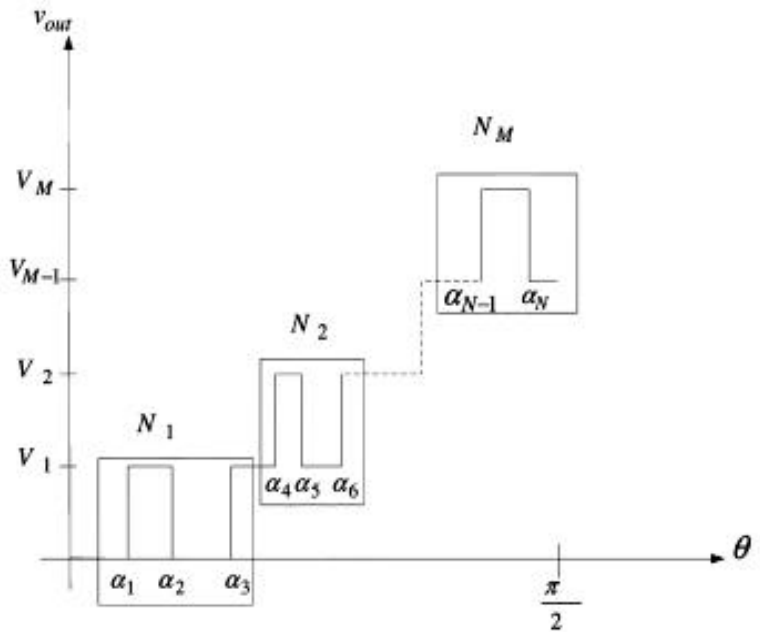


Fig. 4 Voltage output waveform

Equation (7) and (8) shows the voltage output that composed from many signals in different amplitudes and different frequencies. The amplitudes depend on n_{th} harmonic order (only odd) and the cosine result of i_{th} switching angle, and the frequency depends on n_{th} harmonic order. If the voltage output has a fundamental frequency amplitude equal V_f, 3_{th} order frequency amplitude is equal V_3, 5_{th} order frequency amplitude is equal V_5 and so on, the Total Harmonic Distortion (THD) this voltage output can be calculated using equation (9).

$$THD = \frac{\sqrt{V_3^2+V_5^2+V_7^2+\cdots.+V_n^2}}{V_f} X100\% \qquad (9)$$

The different voltages in odd harmonics frequencies also produce different effective voltage and power loss. Different load also results different current THD and other parameter.

3. METHOD

3.1 System Configuration

Block diagram of the simulation system shown at Fig. 5. The system consists of a reference signal, a triangle waveform generator within variable frequency, CMLI unit, and load and CBPWM control unit. A reference signal is a sin signal generator, which frequency similar to electric system used, as an example is 50Hz or 60 Hz. The amplitude of this signal is ten times of carrier signal amplitude. Ten carrier signals within the triangle waveform and variable frequency will be formed in different bias. Reference signal and ten triangle carrier signals then supplied to the control unit. These eleven signals will be changed in the twenty trigger signals to apply to power electronic devices of CMLI unit. In the CMLI, five DC powers converted to AC power and then supply to resistive load or inductive load.

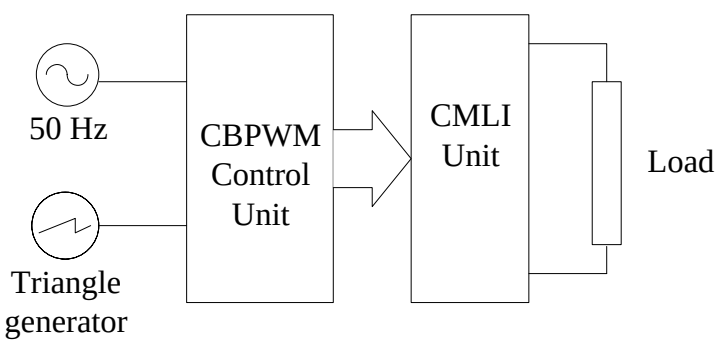


Fig. 5 System configuration

3.2. Development of Simulation Circuit

Fig. 6 show simulation circuit of 11 levels CMLI. In this circuit there are five CBPWM control unit, five H-bridge inverters, five DC powers, a resistive/ inductive load and some signal processor like scopes, voltage measurement, etc. This simulation circuit built using Matlab Simulink [10].

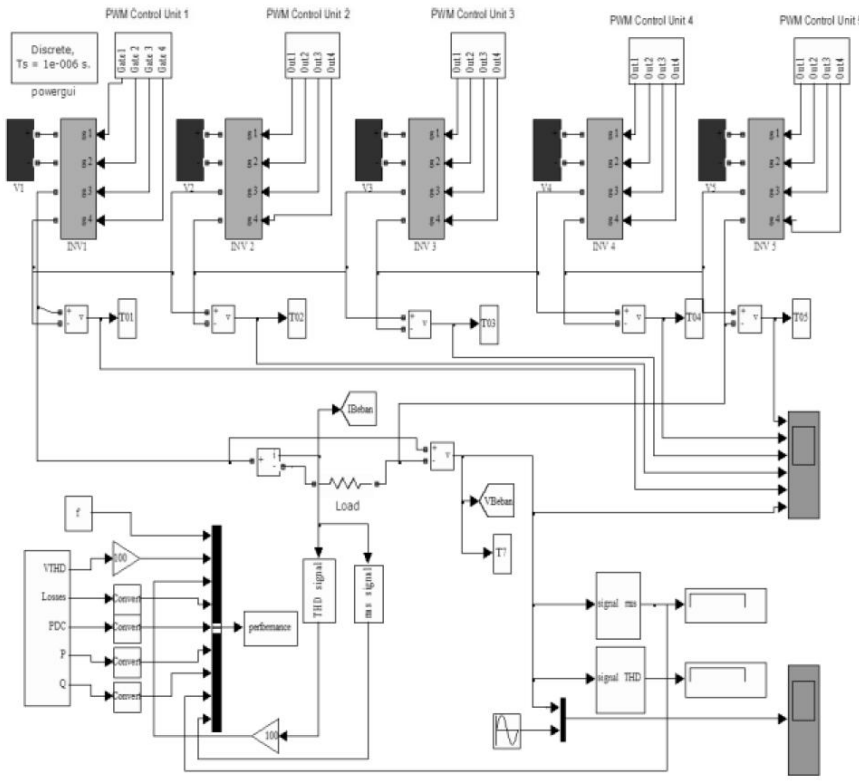


Fig. 6 Simulation circuit

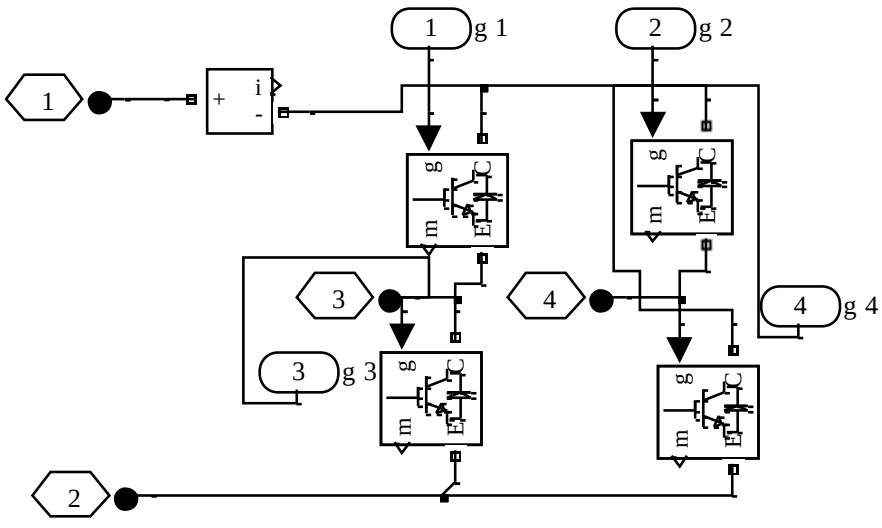


Fig. 7 H-Bridge circuit (INV1-INV5)

H-bridge inverters, in figure 6 called INV1 until INV5, built using four IGBTs as shown in Fig. 7. Fig. 8 show general CBPWM control unit circuit. This unit consists two mayor components, Gate trigger generator (Fig. 9) and Zero gate generator (Fig. 10). Gate trigger generator generates four pulses on each H-Bridges inverter. In the zero condition or if H-Bridges inverter not generate power, pulses must be converted to trigger for two switches in the 0 output as descripted in Table 1. It is done at the zero gate generator.

Each Gate trigger generator has different triangle waveform. Triangle generator on CBPWM control unit 1 until 5 has parameter output value:

[V2+V3+V4+V5 V1+V2+V3+V4+V5 V1+V2+V3+V4+V5 V2+V3+V4+V5]; [V3+V4+V5 V2+V3+V4+V5 V2+V3+V4+V5 V3+V4+V5]; [V4+V5 V3+V4+V5 V3+V4+V5 V4+V5]; [V5 V4+V5 V4+V5 V5]; [0 V5 V5 0] and time value (1/f)*[0 0.5 0.5 1] for all Triangle generator. V1 until V5 are DC sources of CMLI and f is the frequency of sine reference signal. In this case, V1 to V5 and f determined

using m-file program in the Matlab command window. Using this method, the variation of voltage (to make CMLI asymmetric) and frequency can be more easily performed.

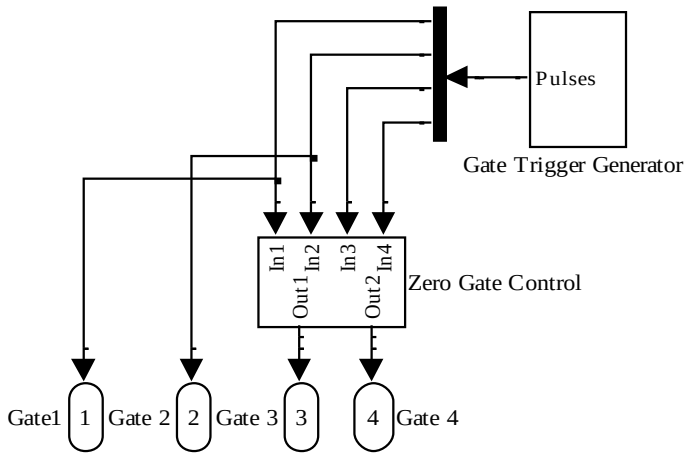


Fig. 8 Control unit circuit

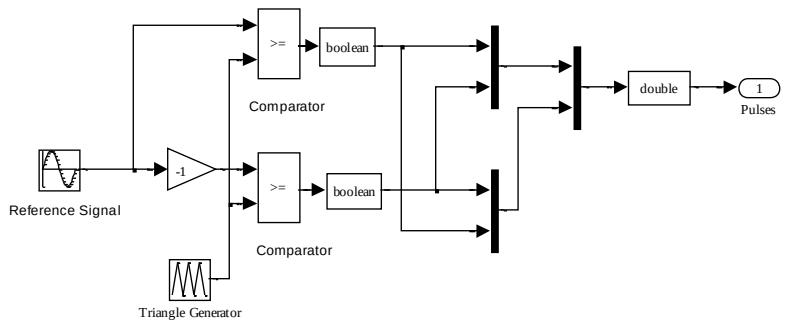


Fig. 9 Gate trigger generator

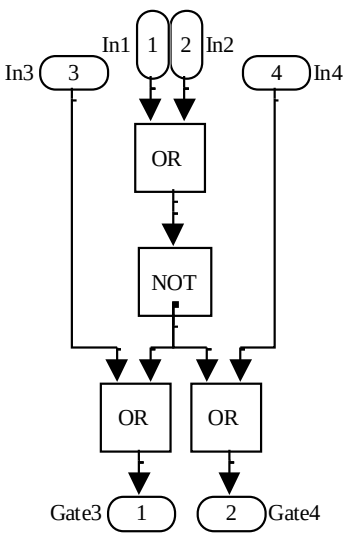


Fig. 10 Zero gate control

4. RESULTS AND DISCUSSIONS

4.1 CBPWM Waveform Verification

Fig. 11 show input signals of control unit 1 and gate signal for power device of highest H-Bridge in the simulation circuit. If the sine reference higher than triangle signals and zero gate control produce connection, gate signal for power devices will produce a high logic (1). The frequency of the reference signal is 50 Hz and the frequency of triangle signals are 500 Hz.

In the time between 0 s to 0.0034 s of this figure, Gate 3 and Gate 4 are in High state. It is mean that highest H-Bridge in 0 volts and only continue current from other H-Bridges. In the time between 0.0034 s to 0.065 s, this H-Bridge produces a voltage or builds a series connection of DC source. Between 0.065 s to 0.013 s, this H-Bridge is at 0 volts again. In the time 0.013 s to 0.016 s, this H-Bridge produce voltage or build a series connection of DC source, but in alternate direction, and finally at the time 0.016 to 0.02, this H-Bridge in 0 volts again. The incident will be repeated from the beginning. Fig. 12 show output voltage on H bridge and on CMLI.

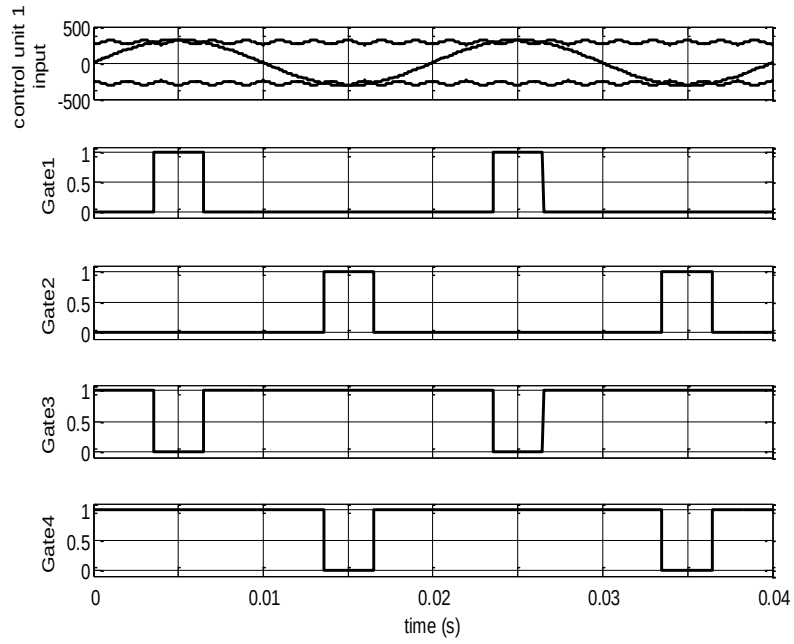


Fig. 11 Control unit 1 signal

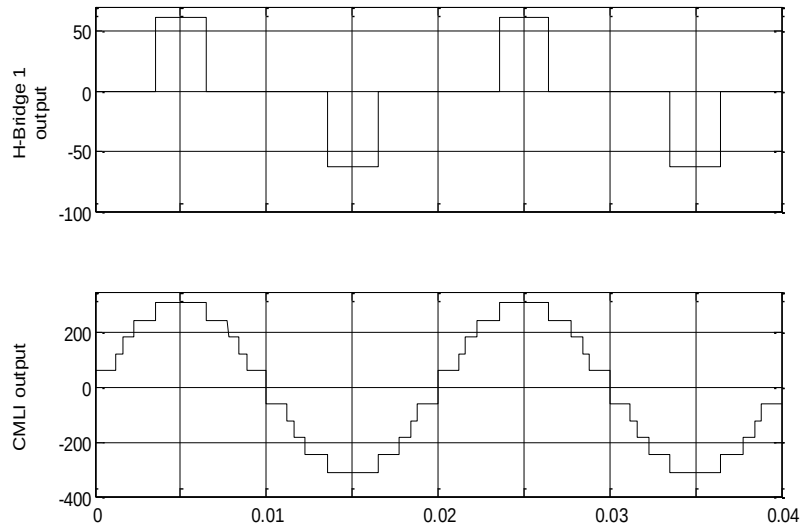


Fig. 12 H-Bridge 1 output and CMLI output

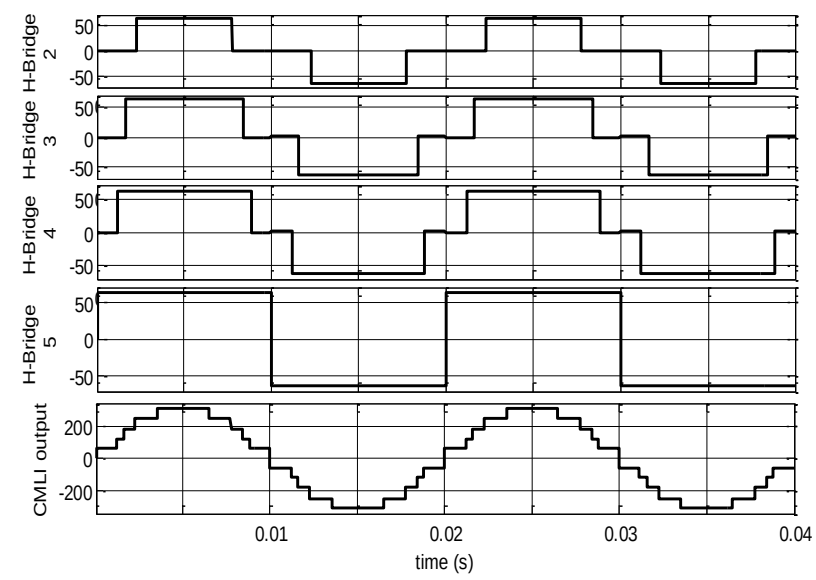


Fig. 13 H-Bridge 2-5 output and CMLI output

In the different carrier frequency, verification of CBPWM also obtains correct waveform. Fig. 14 shows H-Bridge output and CMLI output in the carrier frequency 5000 Hz and sine reference in the 50 Hz.

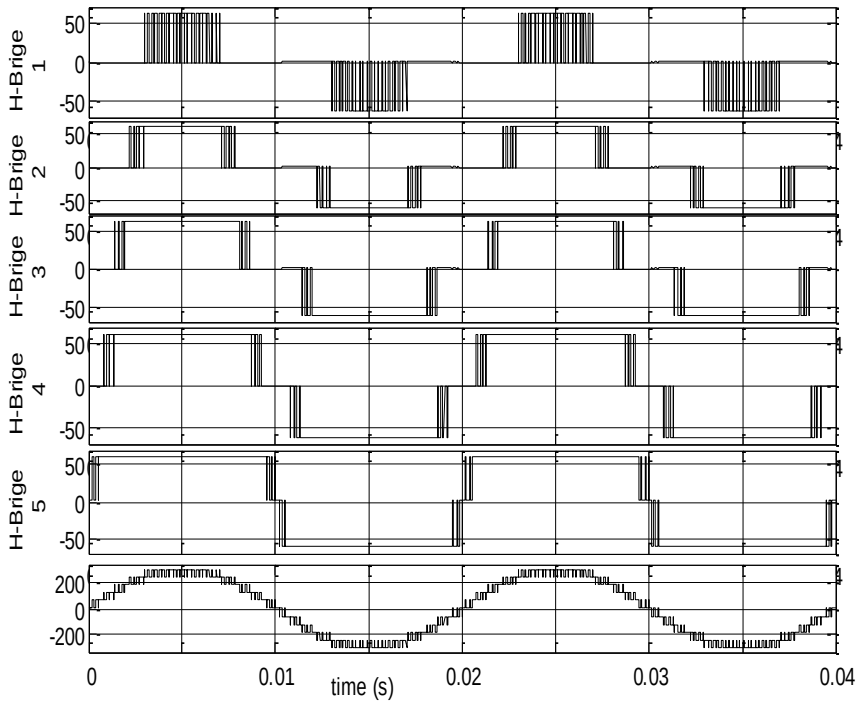


Fig. 14 H-Bridges output and CMLI output at carrier frequency 5000 Hz

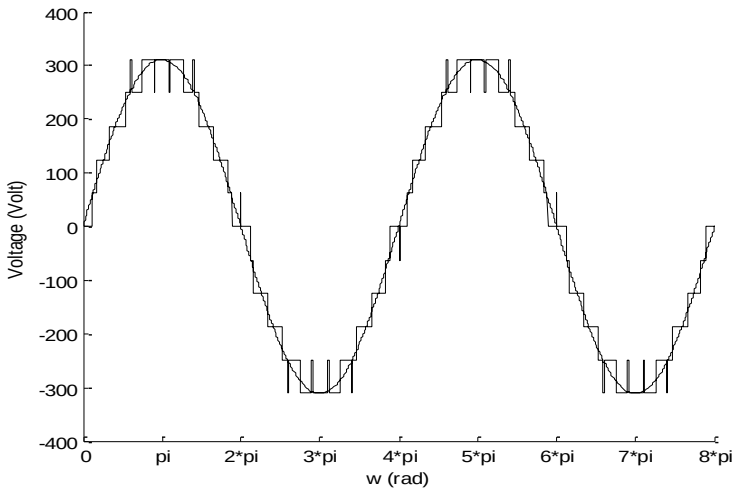


Fig. 15 CMLI output using carrier 1000 Hz

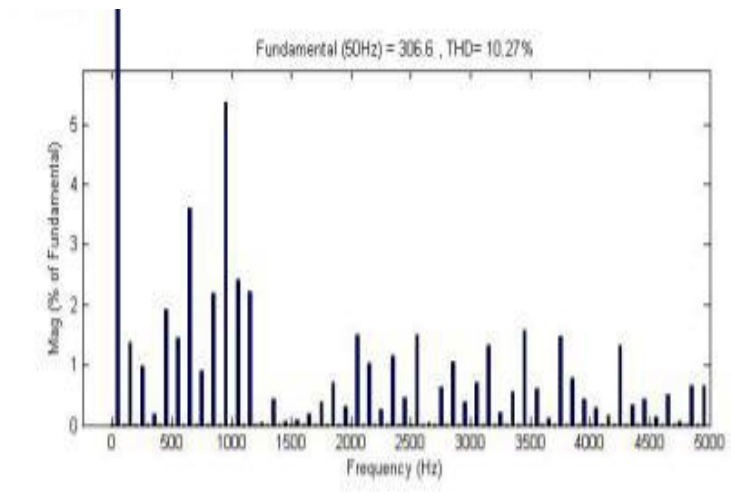


Fig. 16 Voltage frequency spectrum using carrier 1000 Hz

4.2 Power Quality Measurement

In the simulation, power quality measurement using Total Harmonic Distortion function block parameter. The measurements were performed for voltage THD and current THD. If the carrier frequency is 1000 Hz and each DC sauce is 62.2 V, so the output voltage of 11 levels CMLI is shown in Fig. 15 and the frequency spectrum and THD is shown in Fig.16. If the carrier frequency modified to become 500 Hz and the DC sources remains as before, so output voltage of CMLI is shown in Fig. 17 and the frequency spectrum and THD is shown in Fig. 18.

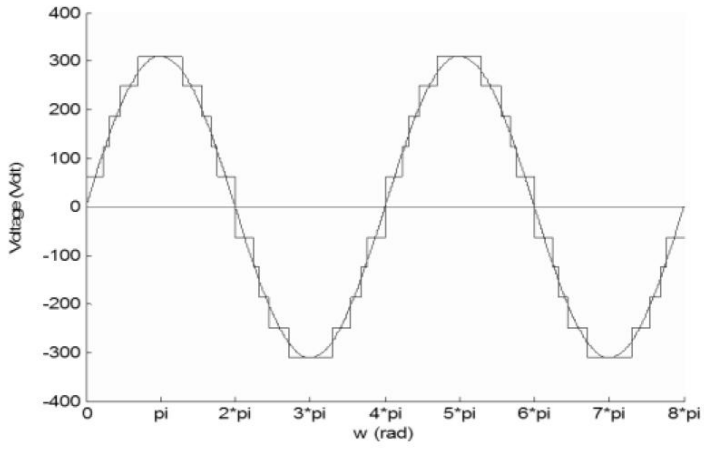


Fig. 17 CMLI output using carrier 500 Hz

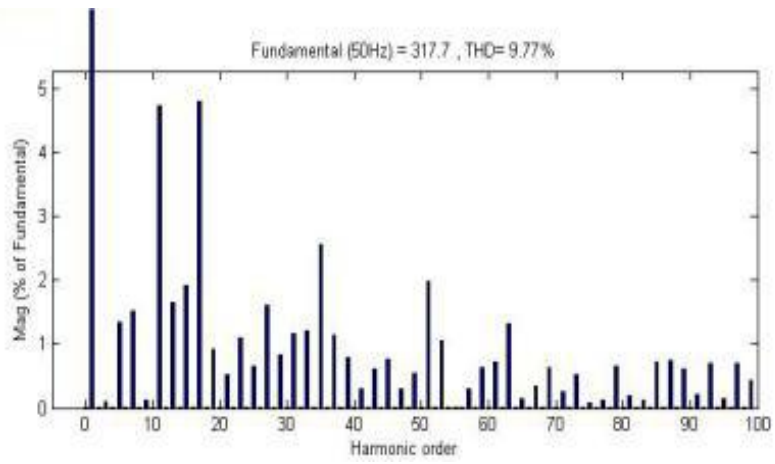


Fig. 18 Voltage frequency spectrum using carrier 500 Hz

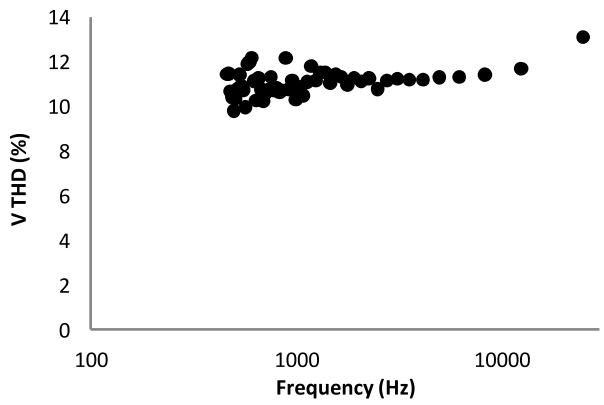


Fig. 19 Voltage THD and carrier frequency relationship for resistive load

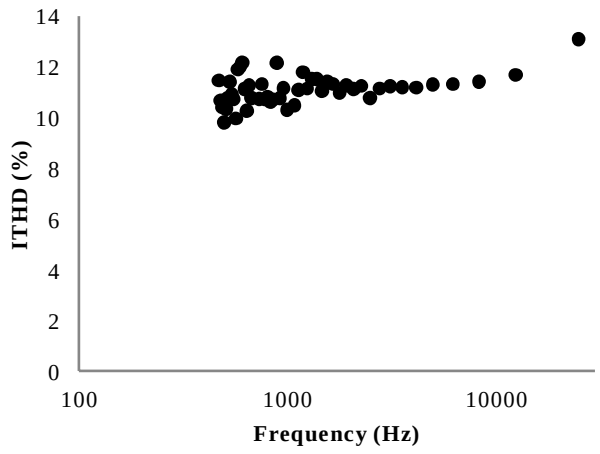


Fig. 20 Current THD and carrier frequency relationship for resistive load

For carrier frequencies varied from 300 Hz to 5000 Hz, voltage THD and carrier frequency relationship for resistive load is shown in Fig. 19, while current THD and carrier frequency relationship for resistive load is shown in Fig. 20. In the inductive load, voltage THD similar to voltage THD in the resistive load, but for current THD, the value of THD will be decreased if the value of inductive load increased.

5. CONCLUSIONS

In this paper a simulation circuit of CBPWM for CMLI circuit designed using Matlab Simulink. Using the proposed design, the CBPWM system for CMLI easily made and easily varied. So, in the next time CMLI can be optimized by DC sources, carrier waveform and frequencies, number of levels, etc.

Verification using output waveform show the simulation circuit is accordance with the theory. In the experimental measurements and in the varied career frequency, 11 levels CMLI has best power quality when the carrier frequency is 10 times of reference frequency or sine reference. At this condition the voltage THD has the smallest value that is 9.77%. While the current THD, is strongly influenced by the type of load. If the load used is a resistive load, the current THD is equal to the voltage THD. But if the load is inductive load, the current THD will be smaller than the voltage THD. The greater the inductive load, will be obtain the smaller value of current THD.

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