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# **TELKOMNIKA**

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Redaksi menerima tulisan ilmiah dalam bidang teknik elektro  
terutama bidang telekomunikasi, komputasi, elektronika, dan kendali

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# IMPROVED VOLTAGE OF CASCADED INVERTERS USING SINE QUANTIZATION PROGRESSION

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## Abstrak

Metode-metode inverter multi level kaskoda (CMLI) yang ada hanya meningkatkan kualitas daya tetapi memiliki tegangan keluaran yang rendah, jika tegangan DC dibatasi oleh rating tegangan semikonduktor daya. Untuk meningkatkan amplituda tegangan keluaran CMLI, makalah ini mengusulkan pola urutan penyaklaran tegangan DC yang baru. Pola urutan tersebut didasarkan pada metode kuantisasi atau sine quantization method (SQM), yang penentuan urutan tegangan DC-nya diperoleh dari pen-diskret-an amplitudo fungsi gelombang sinus. Metode tersebut juga dikolaborasi dengan metode sisa luas sama (SERAM) untuk meminimalkan distorsi harmonisa total atau total harmonics distortions (THD). Suatu inverter kaskoda fase tunggal yang didalamnya berisi inverter sejumlah jembatan H disimulasikan dan diimplementasikan untuk memverifikasi metode yang diajukan. Amplitudo tegangan keluaran dan THD hasil simulasi dan eksperimen menunjukkan bahwa urutan pola kuantisasi sinus menghasilkan tegangan keluaran yang lebih tinggi bila dibanding dengan pola urutan DC lain, dengan kualitas daya atau THD berada pada batasan yang masih bisa diterima. Amplitudo tegangan keluaran memiliki fungsi yang linier dengan gradien 0,6665 untuk tiap kenaikan satu inverter jembatan H yang ditambahkan, dan memiliki penurunan THD dengan fungsi eksponensial dengan nilai yang kurang dari 5%.

**Kata kunci:** CMLI, inverter multilevel, SERAM, THD

## Abstract

The previous methods of cascaded multilevel inverter (CMLI) can improve power quality but the methods have low voltage output if the DC voltages limited by the voltage rating of power semiconductor. To improve the amplitude of CMLI output voltage, this paper proposes a new DC voltage progression. The progression based on sine quantization method (SQM), which determines a sequence of DC voltages from discrete amplitudes of sine wave function. The method also collaborates with step equal residual area method (SERAM) to minimized total harmonics distortions (THD). A single-phase CMLI that consist four H-Bridges simulated and implemented to verify the methods. Amplitude output voltage and THD results of simulations and experiments indicate that the sine quantization progression produce the highest output voltage than other DC voltage progressions, with power quality or THD in the accepted region. The amplitude of output voltage have linier function with amplitude equal 0.6665 times of H-Bridges numbers and have exponential function of THD with value below 5%.

**Keywords:** CMLI, multilevel inverter, SERAM, THD

## 1. INTRODUCTION

Recently the multilevel inverter (MLI) is the most popular dc to ac converters for high voltage and high power in the power industry. The general structure of this MLI is to synthesize a sinusoidal voltage from several levels of voltages [1]-[4]. There are three well-known topologies; diode-clamps, flying capacitor, and cascaded multilevel inverter (CMLI) [4]-[8]. Diode clamp and flying capacitor are MLI with common dc sources. These inverters use capacitors in series to divide the dc bus voltage in to a set of voltage levels. While, the CMLI consists several H-bridge inverter units, and separated DC sources.