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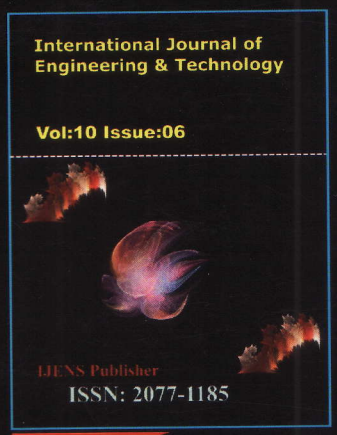

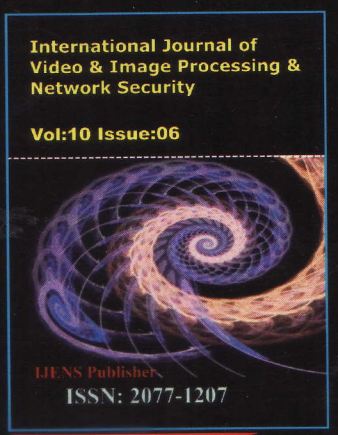

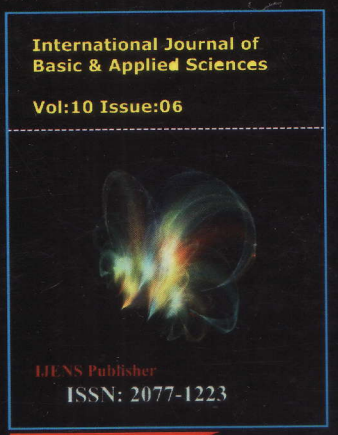

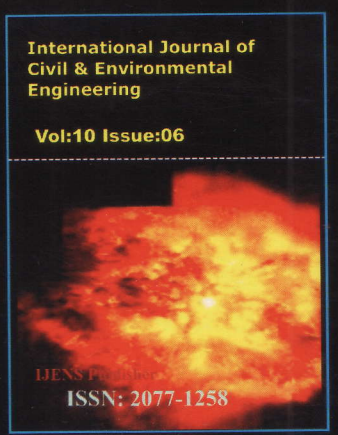

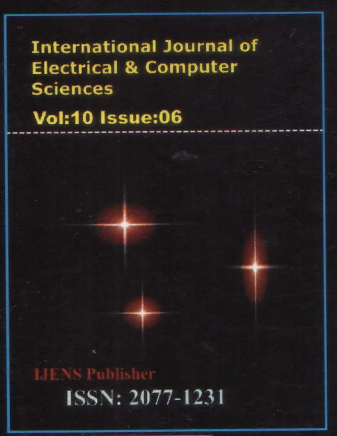

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Advanced Carrier Based Pulse Width Modulation in Asymmetric Cascaded Multilevel Inverter

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Abstract –This paper proposes a new scheme Pulse Width Modulation (PWM) to overcome low performances of conventional PWM control strategy in Cascaded Multilevel Inverter (ACMLI). This scheme advance conventional Carrier-Based PWM (CBPWM) using triangle carrier in different amplitudes. By this scheme ACMLI can control by PWM that according to dc voltage amplitude used and finally the Total Harmonics Distortions (THD) can reduce to the settle standard. Simulation using Matlab Simulink used to verify the performance and result simulation shown than this proposed scheme can reach the goals.

Key word- asymmetric cascaded multilevel inverter, multi carrier pulse width modulation, power quality, total harmonic distortion.

I. INTRODUCTION

The multilevel inverter [MLI] is a promising inverter topology for high voltage and high power applications [1]. This inverter synthesizes several different levels of DC voltages to produce a staircase (stepped) that approaches the pure sine waveform [3-9]. Its have high power quality waveforms, lower voltage ratings of devices, lower harmonic distortion, lower switching frequency and losses, higher efficiency, reduction of dv/dt stresses and gives the possibility of working with low speed semiconductors if its comparison with the two-levels inverters. Numerous of MLI topologies and modulation techniques have been introduced and studied extensively, but most popular MLI topology is Diode Clamp, Flying Capacitor and Cascaded Multilevel Inverter (CMLI). In this paper we use a CMLI that consist ot some H-Bridge inverters and with un-equal DC. Its also namely Asymmetric Cascaded Nultilevel Inverter (ACMLI). Its most implemented because this inverter more modular and simple construction and have other advantages than Diode clamp and flying capacitor [7].

There are many modulation techniques to control this inverter, such as Selected Harmonics Elimination or Optimized Harmonic Stepped-Waveform (OHSW), Space Vector PWM (SVPWM) and Carrier-Based PWM (CBPWM). Among thes modulation CBPWM is the most used for multilevel inverter, brcause it have simple logical and easy to implemented. But if CBPWM used in the ACMLI, there is a problems, that is its have low power quality performance, so many method to adjust this controller find in many papers in the last decade.

To solve this problem, this paper propose a new scheme, which namely Advance Pulse Width Modulations (APWM). This scheme on behalf of PWM, but its not use triangle carrier waveform in equal amplitude as like to in the conventional PWM. The frequency and amplitude of triangle modulation must be according to amplitude of DC voltage on each H-Bridges inverter .

II. ACMLI

CMLI proposed to solve all the problems of the multilevel inverters as well as conventional multi pulse (or PWM) inverters [5-7]. CMLI eliminates the excessively large number of bulky transformers required by conventional multi pulse inverters, the clamping diodes required by multilevel diode clamped inverters, and the flying capacitors required by multilevel flying capacitor inverters.

CMLI consists a series connection of multiple H-bridge inverters. Each H-bridge inverter has the same configuration as a typical single-phase full-bridge inverter [3-4]. CMLI introduces the idea of using separate DC sources to produce an AC voltage waveform. Each H-bridge inverter is connected to its own DC source. By cascading the output voltage of each H-bridge inverter, a stepped voltage waveform is produced [5-7]. If the number of H-bridges is N, the voltage output is obtained by summing the output voltage of bridges as shown in equation (1). Fig. 1 shows configuration of CMLI on single-phase.