ISBN: 978-93-80747-97-0 ISSN: 0975-8887

Foundation of Computer Science

International Journal of Computer Applications

November 2010

Vol 10 - Number 6
www.ijcaonline.org

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First Published in the United States of America.

Originated and printed by Foundation of Computer Science Press, New York, USA

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PAPERS

Universal Algorithm Control for Asymmetric Cascaded Multilevel Inverter

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ABSTRACT
Asymmetric Cascaded Multilevel Inverter (ACMLI) was widely studied. Various control strategies have been investigated. However, most of the reported control strategies not discussed how to determinate voltage levels, firing angle, switching-state and other parameters control design. This work was developed a universal algorithm to overcome the problems in the various number of H-Bridges and various DC voltages of ACMLI. The proposed algorithm based on combination theorem and matrix operation. The MATLAB computer program and simulation using MATLAB SIMULINK in the binary, trinary, equal interval, sine quantization and random DC voltage are the methods for verify the proposed algorithm. The results program execution and simulation in the single phase of ACMLI show that the proposed algorithm produces ACMLI control more accurate and faster if compared with previous control strategies.

General Terms
Algorithms, Control, Power Electronics

Keywords
universal algorithm, asymmetric multilevel inverter, voltage levels, firing angle, switching-state.

1. INTRODUCTION
Recently the multilevel inverter (MLI) is the most popular dc to ac converters topology for high voltage and high power in the power industry. The MLI synthesize a sinusoidal voltage from several levels of voltages [1],[4-5].[8],[11]. There are three well-known topologies; diode-clamps, flying capacitor, and cascaded multilevel inverter (CMLI) [2],[5],[7],[9-10]. CMLI had many advantages than others, especially in reduced component, reduced power loss, reduced power stress, reduced frequency switching, reduced electromagnetic interference, increase voltage and power capability and increase power quality [1],[4],[5].[8],[10-11].

In the early development, all of H-Bridge inverters of CMLI have same voltage, and called equal or symmetric CMLI (SCMLI). But in order to improve power quality with provides a large number of output levels without increasing the number of inverters, unequal DC voltages or asymmetric cascaded multilevel inverters (ACMLI) built, where each H-Bridge inverters have different voltages [10]. These voltages can be followed a certain function [4]. The most popular asymmetric CMLI that follow functions are binary (orde-2) and trinary (orde-3) progressions of DC voltages. Others DC progression are equal interval [6] and sine quantization [3]. To implement ACMLI in the various DC voltage progressions and various numbers of H-Bridges, the main problem is control design that consist some control parameters, especially voltage levels, firing angle and switching-state, because nothing researches reported how to determine these parameters.

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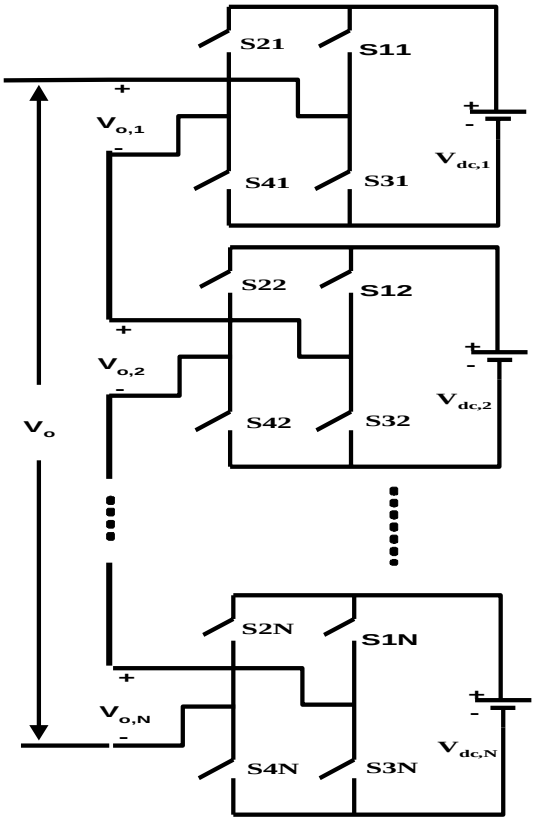


Fig. 1. A Single Phase Asymmetric Cascaded Multilevel Inverter.

This paper proposes an algorithm to determine voltage levels, firing angle and switching-states in the ACMLI to overcome the problem. This algorithm based on effective combination and matrix operations that implemented in the m-file MATLAB program. Result this program then fill in the look up table of single phase ACMLI MATLAB SIMULINK circuit. This algorithm verifies in the five cases of DC voltage progressions,

that is binary, trinary, equal interval, sine quantization and random. Each case investigated in the 2 until 5 numbers of H-Bridges of ACMLI

2. STATE COMBINATIONS OF ACMLI

Basic circuit of single-phase CMLI is show in the fig. 1. Some power devices such as Insulated Gate Bipolar Transistors (IGBT) can realize the switches. If DC voltages in this circuit are equal, this inverter called SCMLI, otherwise these voltages are unequal, the inverter called ACMLI. Switch combinations and output voltages on each H-Bridge of ACMLI shown in table 1. In this table, 1 indicated ON switch condition and 0 indicated OFF state. Each H-Bridges have four switches, so there are 2^4 combinations, but only four combinations that available to produce voltages, because other combinations is no connected (NC) conditions that means not produce voltages, or not permitted (NP) conditions that means short circuit occurred. Four available combinations produce three voltages, 0 V, +Vdcj V and –Vdcj V, where j is jth sequence of H-Bridge. The switch combinations that produce 0 V must be choice of two conditions. So, in the each H-Bridges only have three output voltages and three switching-states.

Using fig. 1, output voltage could express as (1) [1]. If ACMLI have N H-Bridges, there are many output voltages that produce from (1) with each H-Bridges has three varieties and has switching-states that appropriated on the voltages. Each output voltage occurred in ACMLI called voltage levels. Equation (2) and (3) show the probabilities of voltages and switching-states of ACMLI. The switching-states in equation (3) are only in ON condition.

$$V_o(t) = V_{o,1}(t) + V_{o,2}(t) + ... + V_{o,N}(t) \qquad (1)$$

Table 1. Switch states and output voltage of each H-Bridge

Switch states				
S1j	S2j	S3j	S4j	
0	0	0	0	NC
0	0	0	1	NC
0	0	1	0	NC
0	0	1	1	0
0	1	0	0	NC
0	1	0	1	NP
0	1	1	0	-Vdcj
0	1	1	1	NP
1	0	0	0	NC
1	0	0	1	Vdcj
1	0	1	0	NP
1	0	1	1	NP
1	1	0	0	0
1	1	0	1	NP
1	1	1	0	NP
1	1	1	1	NP

In Ref. [1] and [4], the voltage maximum and the number of voltage output levels of ACMLI in the binary and trinary DC voltage progression have discussed and result equation (4) until (7). Different DC voltage progression also have discussed in [3] and [6]. But in these reference and others not discussed how to determine switching-states for the voltage levels. The switching-states usually calculated manually. If there are a lot of H-Bridges and widely vary of the DC voltage used, so count manually will require time, difficult and there are even possible mistakes.

$$Vo = \begin{pmatrix} -V_{0,1} - V_{o,2} - V_{0,3} - ..... - V_{o,N} \\ ..... \\ -V_{o,N-1} - V_{o,N} \\ -V_{o,N} \\ 0 \\ V_{o,N} \\ .V_{o,N-1} + V_{o,N} \\ ..... \\ V_{o,1} + V_{o,2} + ... + V_{o,N} \end{pmatrix} \qquad (2)$$

$$Switching\ States = \begin{pmatrix} S_{21}, S_{31}; S_{22}, S_{32}; S_{23}, S_{33}; .....S_{2N}, S_{3N} \\ ..... \\ S_{31}, S_{41}; S_{32}, S_{32}; .....S_{3N-1}, S_{4N-1}; S_{2N}, S_{3N} \\ S_{31}, S_{41}; S_{32}, S_{42}; S_{33}, S_{43}; .....S_{2N}, S_{3N} \\ S_{31}, S_{41}; S_{32}, S_{42}; S_{33}, S_{43}; .....S_{3N}, S_{4N} \\ S_{31}, S_{41}; S_{32}, S_{42}; S_{33}, S_{43}; .....S_{1N}, S_{4N} \\ S_{31}, S_{41}; S_{32}, S_{42}; .....S_{3N-1}, S_{4N-1}; S_{1N}, S_{4N} \\ ..... \\ S_{11}, S_{41}; S_{12}, S_{42}; S_{13}, S_{43}; .....S_{1N}, S_{4N} \end{pmatrix} \qquad (3)$$

3. PROPOSED ALGORITHM

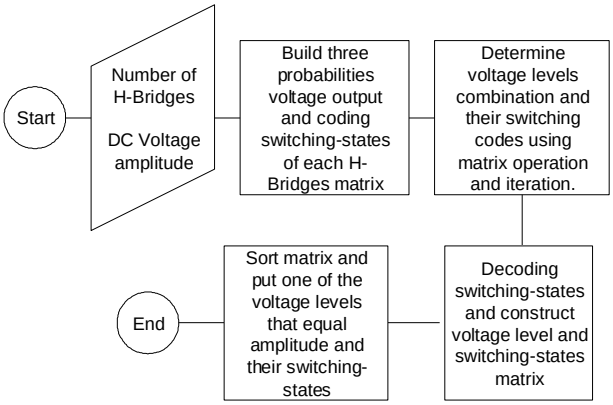
In this paper proposes an algorithm for determine the voltage levels and switching-state as a new method to solve the above problem. Figure 2(a) show flowchart of this algorithm. The main variables in this algorithm are number of H-bridge and DC voltage of ACMLI.

$$Vo,\max = (2^N - 1)Vdc \quad if\ Vdc, j = 2^{j-1}Vdc, j = 1,2,....N \qquad (4)$$

$$Vo,\max = (\frac{3^N - 1}{2})Vdc \quad if\ Vdc, j = 3^{j-1}Vdc, j = 1,2,...N \qquad (5)$$

$$n = 2^{N+1} - 1 \quad if\ Vdc, j = 2^{j-1}Vdc, j = 1,2,....N \qquad (6)$$

$$n = 3^N \quad if\ Vdc, j = 3^{j-1}Vdc, j = 1,2,....N \qquad (7)$$



(a) Flow Chart

```
% Build three probabilities matrix
    V=[-1*Vdc1 -1*Vdc2…-1*VdcN…Vdc1 Vdc2...VdcN 0 0… 0];
    Q =[N123…2123 1123 N914….2914 1914 N034… 2034 1034];

% Determine combination
Vx1=0;Vx2=0;Vx3=0;Vx4=0;….VxN=0;
for i1=1:3*N;
……
 if i1<=5
 V1(:,i1+4)=[];
 V1(:,i1+8)=[];
 Q1(:,i1+4)=[];
 Q1(:,i1+8)=[];
…….
Vout(a)=Vx1+Vx2+Vx3+Vx4+Vx5;
     Q1out(a)=Q1x;
……..
% Sort and put voltage levels
Mx=M;
Ms=sortrows(Mx)';
…….
     for v=1:max-m
     if round(1000*Msr(1,m))==round(1000*Msr(1,v+m))
     Ms(:,v+m-a)=[];
     a=a+1;
% Decoding
if Msx(i,j)==3914
     tabel(i,2+8)=1;
     tabel(i,3+8)=0;
     tabel(i,4+8)=0;
     tabel(i,5+8)=1;
……
end.
```

(b) a part of program

Fig. 2. Flowchart and a part program of algorithm of ACMI

After determined number of H-Bridges and each DC voltage of ACMLI, the next step is build matrix that consist three probabilities voltage output and coding switching-states of each H-Bridges. Example, if DC voltages are V1, V2, and V3, the voltage output matrix is (8) and the coding switching-state matrix is (9).

$$V=[-V1, -V2, -V3, V1, V2, V3, 0, 0, 0] \quad (8)$$

$$Q=[3123,2123,1123,3914,2914,1914,3034,2034,1034] \quad (9)$$

The third step is determined of voltage levels combination and their switching codes using matrix operation. In this step, each H-Bridges only can be presented in one voltage, while others must be eliminated. Example, using (8) and (9) if H-Bridge 1 is in the –V1, so voltage matrix becomes (10) and switching-state matrix become (11). V matrix remains 7 elements, and so Q matrix. Applying the procedure in all of H-Bridges using iteration program, and use (1) and also use recording of switching states, we can determine all of probability voltage levels and switching states.

$$V=[-V1, -V2, -V3, V2, V3, 0, 0] \quad (10)$$

$$Q=[3123,2123,1123,2914,1914,2034,1034] \quad (11)$$

The fourth step is sort result previous step and put one of the voltage levels that equal amplitude. Finally, the switching-states decode in the 1 (ON) or 0 (OFF) state as trigger signal for power electronic devices.

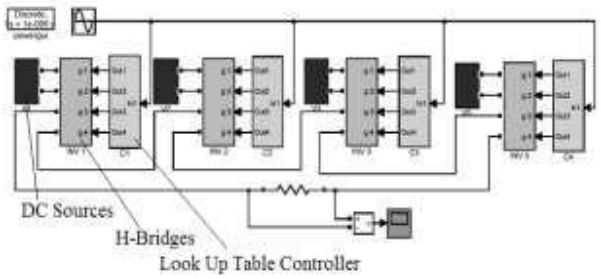


Fig. 3. Simulation circuit.

4. RESULTS AND DISCUSSION

The algorithm then builds in the m-file MATLAB program. Figure 2(b) shows a part of the main program. Final results of the program are voltage levels and switching-state for ACMLI control. To verify the algorithm, the program and simulation applied in five cases of DC voltages progression, that is the binary, trinary, equal interval, sine quantization and random for 2, 3, 4 and 5 H-Bridges. The simulation circuit showed in figure 3.

4.1 Case I: Binary DC voltage progression

In the binary DC voltage progression, ACMLI have voltage in the ratio V1=1, V2=1/2, V3=1/4, V4=1/8, V5=1/16, …… $Vn=1/2^n$. If the highest DC voltage equal 1 p.u (power unit), the results of m-file program in the 2 H-Bridges (only V1 and V2), shown in table 2, where 1 indicate switch in the ON (conduct) and 0 indicate switch in the OFF (open).

Table 2 Voltage levels and switching-states of 2 H-Bridges Binary DC voltage progression of ACMLI.

Voltage levels	Switch states							
	H-Bridges 1				H-Bridge 2			
	S11	S21	S31	S41	S12	S22	S32	S42
-1.5	0	1	1	0	0	1	1	0
-1	0	0	1	1	0	1	1	0
-0.5	0	1	1	0	0	0	1	1
0	0	0	1	1	0	0	1	1
0.5	0	1	1	0	1	0	0	1
1	0	0	1	1	1	0	0	1
1.5	1	0	0	1	1	0	0	1

In the similar method, for 3 (V1, V2 and V3), 4 (V1 to V4) and 5 (V1 to V5) H-Bridges of ACMLI we can determine voltage levels and switching-states (result of the process not shown in this paper), but simulation indicate that m-file program have good solutions. Figure 4 shows the simulation result of binary DC voltage progression in the 2, 3, 4 and 5 H-Bridges using the electric system with frequency 50 Hz, and in the highest DC voltage equal to 1 p.u (power unit).

If this result compare to previous research, it inferential that algorithm result have same the number of output voltage levels and the output voltage maximum. Using algorithm $n=2^{N=1}-1$, equal to result in [1] and so the output voltage maximum, that equal to $(2^N-1)Vdc$.

4.2 Case II: Trinary DC voltage progression.

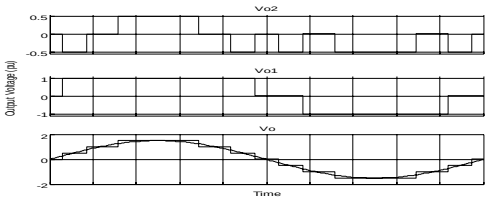
In the trinary DC voltage progression, DC voltages of ACMLI have ratio V1=1, V2=1/3, V3=1/9, V4=1/27, V5=1/81, …… $Vn=1/3^n$. Running the m-fie MATLAB program and simulation circuit using MATLAB SIMULINK, the voltage waveform of 2, 3, 4 and 5 H-Bridges shown in figure 5. This result indicated that the output voltage and switching-states are appropriate with result in the previous research as reported in [1] and [4].

4.3 Case III: Equal Interval DC voltage progression

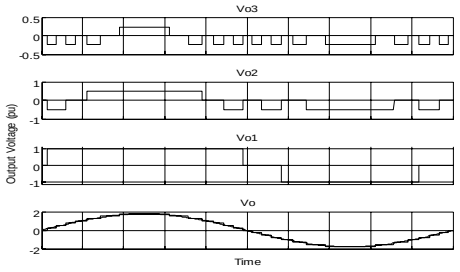
For equal interval DC voltage progression, number of voltage levels, DC voltages, and maximum output voltage calculate using (12) and (13) [10]. If the N=2, V1=1, V2=1/2; N=3, V1=1, V2=2/3, V3=1/3; N=4, V1=1, V2=3/4, V3=1/2, V4=1/3; and N=5, V1=1, V2=4/5, V2=3/5, V3=2/5, V5=1/5. Figure 6 shows output voltage on each H-Bridge and output voltage of ACMLI as result of program and simulation these voltages condition.

4.4 Case IV: Sine Quantization DC voltage progression.

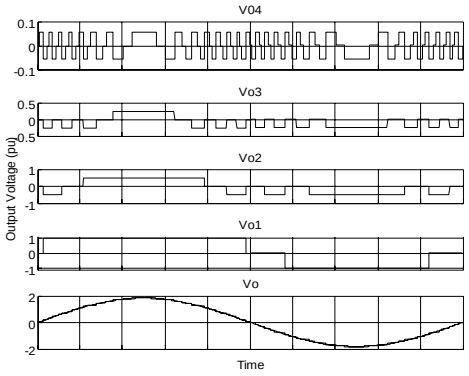
If ACMLI use sine quantization progression [3], each DC voltage can be determined by equation (14). In this equation the voltage of sine wave reference is Vm, the frequency is f, the sequence number of H-Bridge is j and the number of H-Bridge is N). While the maximum output voltage calculate by equation (15). Using proposed algorithm, the simulation result shown in figure 7.



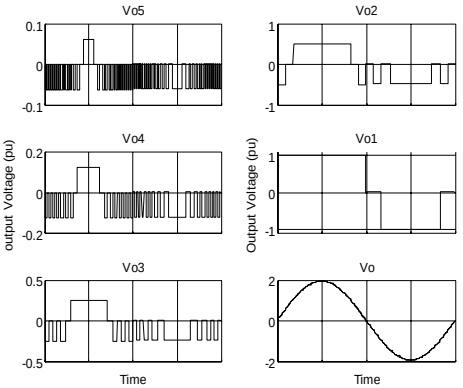
(a) 2 H-Bridges



(b) 3 H-Bridges

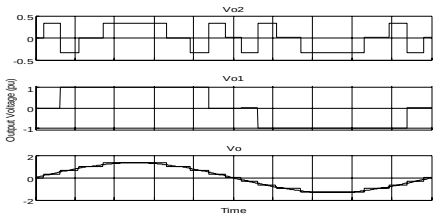


(c) 4 H-Bridges

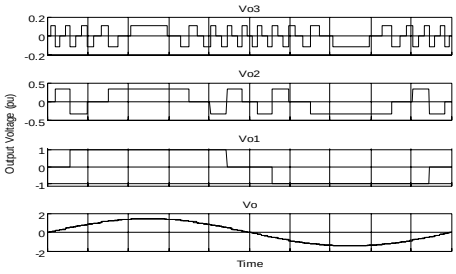


(d) 5 H-Bridges

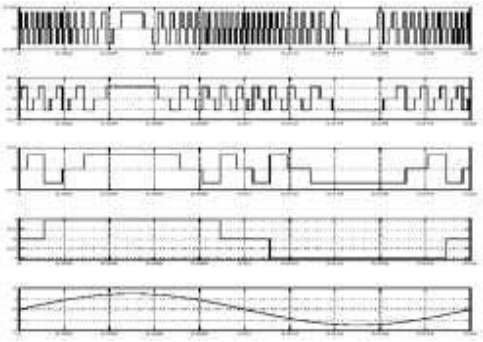
Fig. 4. Voltage waveform of binary DC voltage progression



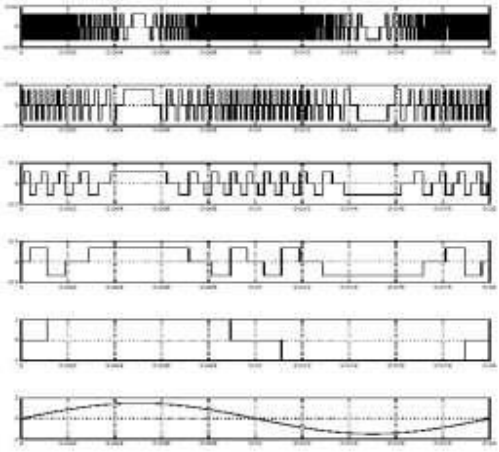
(a) 2 H-Bridges



(b) 3 H-Bridges

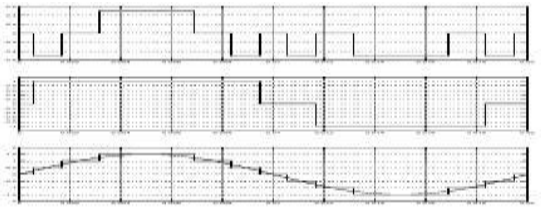


(c) 4 H-Bridges

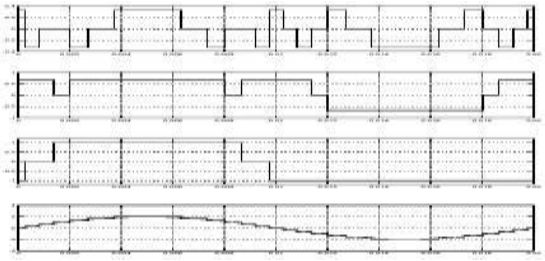


(d) 5 H-Bridges

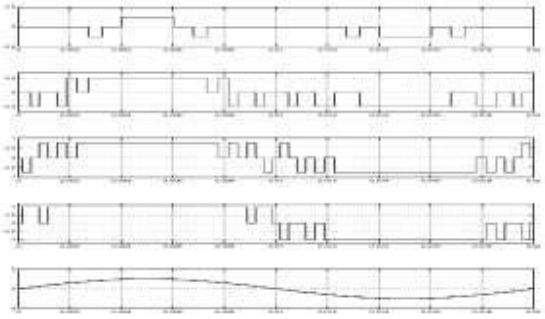
Fig. 5. Voltage waveform of trinary DC voltage progression



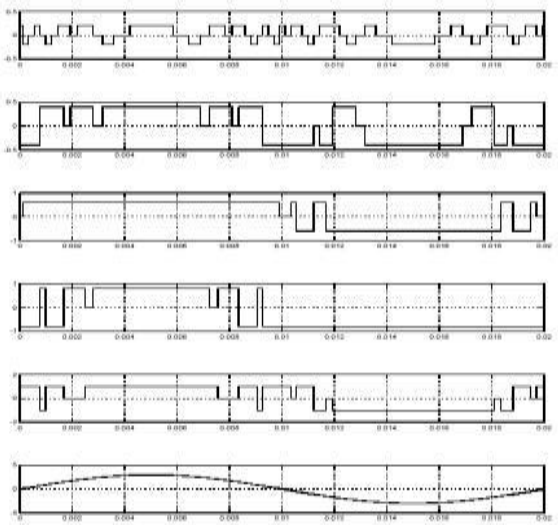
(a) 2 H-Bridges



(b) 3 H-Bridges



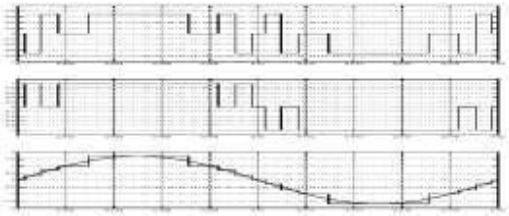
(c) 4 H-Bridges



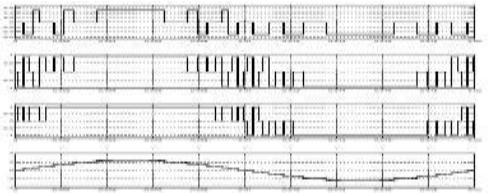
(d) 5 H-Bridges

Fig. 6. Voltage waveform of equal interval DC voltage progression

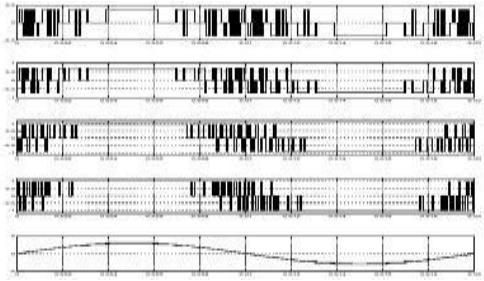
$$V_{dc,j} = V_m \sin(\omega t_j)$$
$$= \sqrt{2}V \sin(2\pi f \frac{(1/f)}{4N} j)$$
$$= \sqrt{2}V \sin(\pi j \frac{1}{2N}) \quad j = 1,2,3...,N \quad (14)$$
$$V_{\max} = \sum_{1}^{N} \sqrt{2}V \sin(\pi j \frac{1}{2N}) \quad j = 1,2,3...,N \quad (15)$$



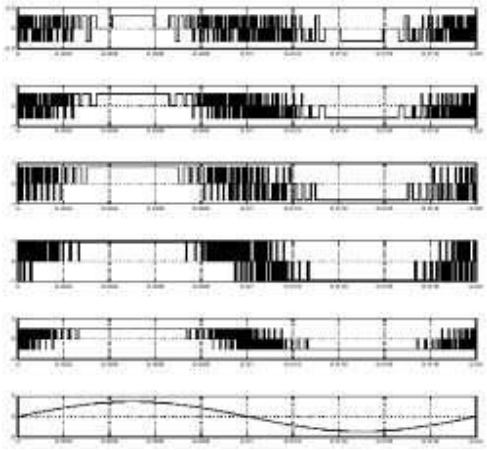
(a) 2 Hbridges



(b) 3 Hbridges

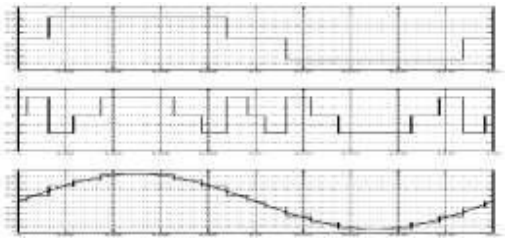


(c) 4 H-Bridges

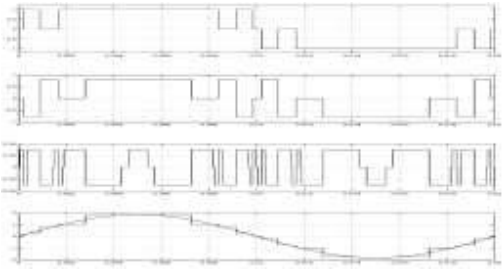


(d) 5 H-Bridges

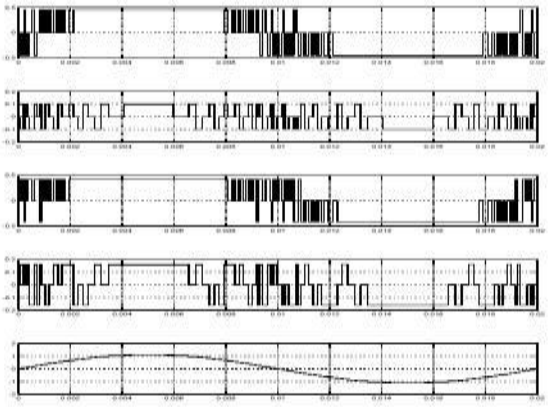
Fig. 7. Voltage waveform of sine quantization DC voltage progression



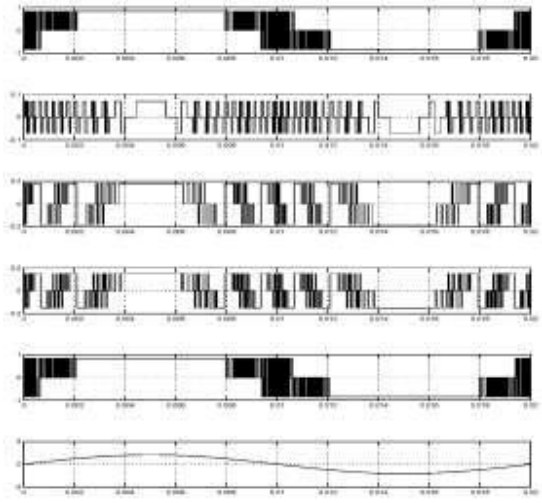
(a) 2 H-Bridges



(b) 3 H-Bridges



(c) 4 H-Bridges



(d) 5 H-Bridges

Fig. 8. Voltage waveform of random DC voltage progression

4.5 Case V: Random DC voltage

Random DC voltages determine using the following matlab program (16). Only Vdc that used that include in the program. In the simulation we use DC Voltages for 2 until 5 H-Bridges as described in (17).

```
DC=randint(1,100,[1,100])/100;
Vdc1=DC(1,1);
Vdc2=DC(1,2);
Vdc3=DC(1,3);
Vdc4=DC(1,4);
Vdc5=DC(1,5);                    (16)
```

```
V1=0.68; V2-0.2
V1=1; V2=0.8; V3=0.03
V1=0.45; V2=0.1; V3=0.42; V4=0.16
V1=0.83; V2=0.07; V3=0.18; V4=0.15; V5=0.84   (17)
```

Simulation using circuit SIMULINK MATLAB, which the content of look up table put from m-file program execution, result output voltages waveform shown in the figure 8.

5. CONCLUSIONS

The m-file program, which represented the proposed algorithm, and verification result use simulation indicate that algorithm had correct solutions, where result of some output voltage levels and switching states in similar with the result of previous researches. So the algorithm can use to serve control design of ACMLI in the various numbers of H-Bridges and various DC voltages quickly and precisely.

The algorithm can develop by integrate with THD elimination/minimization methods to improve power quality. In the future the algorithm also can develop to adaptive control design for fluctuated DC sources like in renewable energy systems.

6. ACKNOWLEDGMENTS

This work is supported the Doctor-Grant 2009, Higher Education General Directorate, the Ministry of National Education, Indonesia.

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